A radio apparatus and a method for reducing interference in a radio apparatus

Field

[0001] The invention relates to a radio apparatus and to reducing interference arising from a clock signal generated in the apparatus.

Background

[0002] Modern electronic radio devices use oscillators to generate clock signals needed in several different parts of the devices. For example, phase lock loops, modulators and demodulators and many digital base band components require clock signals.

[0003] It is typical for oscillators that in addition to the actual clock signal they also produce different harmonic frequencies. This is a feature of all oscillators. Harmonics are multiplies of the actual clock signal frequency. Harmonics caused by clock signals may cause problems in sensitive radio frequency parts in radio devices, such as transceivers in cellular systems. For example, in transceivers of GSM cellular system, VCTCXO Oscillators are widely used (as 13MHz or 26MHz reference clocks, for example). Harmonics arising from the clock signal can be seen as reduced receiver sensitivity on some radio channels or as interference peaks in the receiver band noise spectrum.

[0004] Prior art offers some solutions to this problem. The alternatives have been filtering, tuning of the groundings on a printed board (PWB) and maximizing the isolation between the clock and sensitive parts. These solutions have so far provided only partial solution to the problem. It is not possible to isolate the harmonic signals completely from the radio frequency parts. Furthermore, this problem will get worse when development of device design moves towards so called system on chip (SoC) solutions where more and more blocks are placed very close to each other and isolation between noisy and sensitive blocks is reduced.

Brief description of the invention

[0005] An object of the invention is to provide an improved solution to reducing interference in a radio apparatus. According to an embodiment of the invention, there is provided a radio apparatus comprising means for communicating on at least one radio frequency channel, means for generating a

clock signal, means for measuring interference arising from the harmonic frequencies of the clock signal on the given radio channel, and means for controlling the pulse width of the clock signal on the basis of the measurement.

[0006] According to another embodiment of the invention, there is provided a radio apparatus arranged to communicate on at least one radio frequency channel, comprising a clock signal generator, a radio frequency part and a controller arranged to measure interference arising from the harmonic frequencies of the clock signal on the given radio channel, and a controller for controlling the pulse width of the clock signal on the basis of the measurement.

[0007] According to another embodiment of the invention, there is provided an arrangement for reducing interference in a radio apparatus comprising means for communicating on at least one radio frequency channel, and means for generating a clock signal, the arrangement comprising: means for measuring interference arising from the harmonic frequencies of the clock signal on the given radio channel, and means for controlling the pulse width of the clock signal on the basis of the measurement.

[0008] According to another embodiment of the invention, there is provided a method of reducing interference in a radio apparatus, the method comprising generating a clock signal; measuring interference arising from the harmonic frequencies of the clock signal on a given radio channel, controlling the pulse width of the clock signal on the basis of the measurement.

[0009] The method and system of the invention provide several advantages. By adjusting the pulse width of the clock signal the level of the harmonic signals can also be adjusted. Interference peaks in given radio channels can thus be reduced. Requirements for isolation and filtering can also be reduced. Therefore it is also easier to integrate more functionality onto a single chip (SoC). Radio frequency performance is improved in general.

List of drawings

[0010] In the following, the invention will be described in greater detail with reference to the preferred embodiments and the accompanying drawings, in which

[0011] Figure 1 illustrates square waves with different pulse widths;

[0012] Figures 2A and 2B illustrate the levels of some harmonics;

[0013] Figure 3 illustrates an example of a radio apparatus;

[0014] Figure 4 illustrates an example of a pulse width control;

[0015] Figure 5 illustrates a flowchart of an embodiment.

Description of embodiments

[0016] Figure 1 illustrates square waves with different pulse widths. Clock signals are typically generated as square waves. A square wave 100 has two cycles: a duty cycle 102 when the pulse signal is up and a rest cycle 104 when the pulse signal is down. In the square wave 100 both cycles are of the same length. It can thus be said that the square wave 100 has a duty cycle of 0.5. In a square wave 106 the duty cycle 102 is shorter compared with the rest cycle 104. The duty cycle of the square wave 104 is in this case smaller than 0.5. Respectively, as in the square wave 106 the duty cycle 102 is longer compared with the rest cycle 104, the duty cycle of the square wave 104 is greater than 0.5.

[0017] The harmonics of a square wave signal are dependent on the pulse width or the duty cycle of the signal. For example, a 0.5-duty-cycle signal has only odd harmonic frequencies. In figures 2A and 2B the levels of some harmonics are presented based on Fourier transform of an asymmetric pulse train. Fourier coefficients for asymmetric pulse train can be calculated as

$$|X_n| = \frac{A\tau}{T_0}\left|\sin c(nf_0\tau)\right|, n = 0, \pm 1, \pm 2, \ldots,$$

[0018] where τ = pulse width, T_0 = signal period. A denotes signal amplitude and f_0 denotes frequency. Figure 2A presents odd harmonics as a function of the pulse width. The x-axis shows the duty cycle from 0.0 to 1.0 and the y-axis shows the Fourier coefficients for odd harmonic frequencies. The figure illustrates 3rd harmonics 200, 5th harmonics 202, 7th harmonics 204 and 9th harmonics 206.

[0019] Respectively, Figure 2B presents even harmonics as a function of the pulse width. The figure illustrates 4th harmonics 208, 6th harmonics 210, 8th harmonics 212, 10th harmonics 214 and 20th harmonics 216.

[0020] It can be seen that the level of harmonics is changed in respect to the pulse width. The frequency of the notches increases with higher order harmonics. The duty cycle of 0.5 gives minimum level for all even harmonics.

[0021] Figure 3 illustrates an example of a radio apparatus applying an embodiment of the invention. The apparatus comprises an analog part 336 and a digital part 338. The apparatus comprises an antenna 300, which receives a signal, which is taken to a band pass filter 302 and a low noise ampli-

fier 304. The signal at the output of the amplifier is divided into two branches 306, 308. The receiver comprises a phase lock loop 310, which controls a voltage-controlled oscillator 312. The output of the oscillator is forwarded to a mixer 314 of the branch 306 via a phase shifter 318 and directly to a mixer 316 of the branch 308. In the mixers 314, 316 the signal from the output of the amplifier 304 is multiplied by the oscillator signal, thus performing a down-conversion to an intermediate or a base band frequency. From the mixers the down-converted signal is taken to low pass filters 320, 322, and to amplifiers 324, 326. The amplified signals are taken to a converter 328, where the signals from the branches are converted to the digital form in analogue-to-digital converters 330, 332.

[0022] From the converter 328 the digital signals are forwarded to a digital controller 334. The controller further processes the received signals. The controller also controls the operation of the receiver. The apparatus is able to communicate on different radio channels. The controller 328 may control the operation of the voltage-controlled oscillator via the phase locked loop in such a way that the desired radio channel frequency is down-converted in the mixers 314, 316. The controller may be realized using a digital signal processor, a general processor or discrete components, and suitable software.

[0023] The apparatus described above may also comprise a transmitter part. However, these are not described for simplicity. The apparatus may thus be a receiver, a transmitter or a transceiver.

[0024] The apparatus comprises at least one oscillator 340, which generates a clock signal. The generated clock signal 342, which at the output of the oscillator 340 is typically a sinusoidal signal, is taken to a buffer 344, which converts the signal into a square wave format. The square wave clock signal 346 is taken to the phase lock loop 310 and the controller 334 as an input signal.

[0025] In an embodiment of the invention the controller 338 of the apparatus controls the pulse width of the clock signal. The digital control signal 348 of the converter is converted into an analog form in a D/A-converter 350 and the output of the converter 350 is connected to the buffer 344.

[0026] Figure 4 illustrates an example of the buffer control, where the pulse width is implemented by changing an offset in the buffer input. The output signal 342 from the oscillator 340 is taken to the buffer 344 as an input. The D/A-converter 350 receives a control signal 348 from the controller. The

signal level indicated by the signal corresponds to an offset voltage of the buffer. The D/A converter outputs an analogue offset signal in a differential form 400, 402 to the buffer 342. The differential form comprises the required offset voltage O_o in a positive and negative form ($+O_o$ and $-O_o$). The buffer converts the sinusoidal oscillator signal 342 into a square wave 346.

[0027] The offset voltage control may also be implemented in a single ended form, where the D/A-converter 350 outputs only one voltage value $+O_o$, which is taken against common ground voltage.

[0028] Figure 5 illustrates a flowchart of an embodiment of the invention applied in a receiver apparatus. First, in step 500, the receiver tunes to a radio channel and starts reception on the channel. Tuning means, in this case, changing the output frequency of the voltage-controlled oscillator 312 to the given frequency. Next, the receiver measures the interference arising from the harmonics on the given channel. In an embodiment of the invention no actual signal is transmitted on the radio channel at the time of the measurement. The received signal thus basically comprises noise. The received signal is processed normally in the receiver, that is, filtered, amplified, divided into two branches, and processed in the branches as described above.

[0029] The digitized signal form the output of the converter 328 is taken into the base band controller 334, which is arranged to detect interference peaks in the signal in step 502. On the basis of the found interference peaks the controller generates 504 a control signal 348 for the pulse width control. The signal is then converted to an analog signal in the converter 350 and passed to the clock signal buffer 344 where the pulse width of the signal is adjusted 506 on the basis of the signal.

[0030] This measurement and control process may be repeated iteratively until the interference peaks have been sufficiently eliminated. In an embodiment of the invention the controller may have reference thresholds, below which the interference peaks should be adjusted.

[0031] In an embodiment the above-described measurement and control process is performed each time before the radio apparatus begins communication on a given radio channel. For example, the control process may be performed before the radio apparatus begins a phone call on the given frequency.

[0032] In an embodiment, where the communication uses a frame structure, such as the frame structure of the GSM cellular system (Global Sys-

tem for Mobile communication), the above described measurement and control process is performed before each frame. Thus the interference arising from the harmonics may be efficiently kept below the desired limits. Performing the control on a frame-by-frame basis has the advantage that the frequency hopping used in GSM systems does not disturb the control process.

[0033] Even though the invention is described above with reference to an example according to the accompanying drawings, it is clear that the invention is not restricted thereto but it can be modified in several ways within the scope of the appended claims.